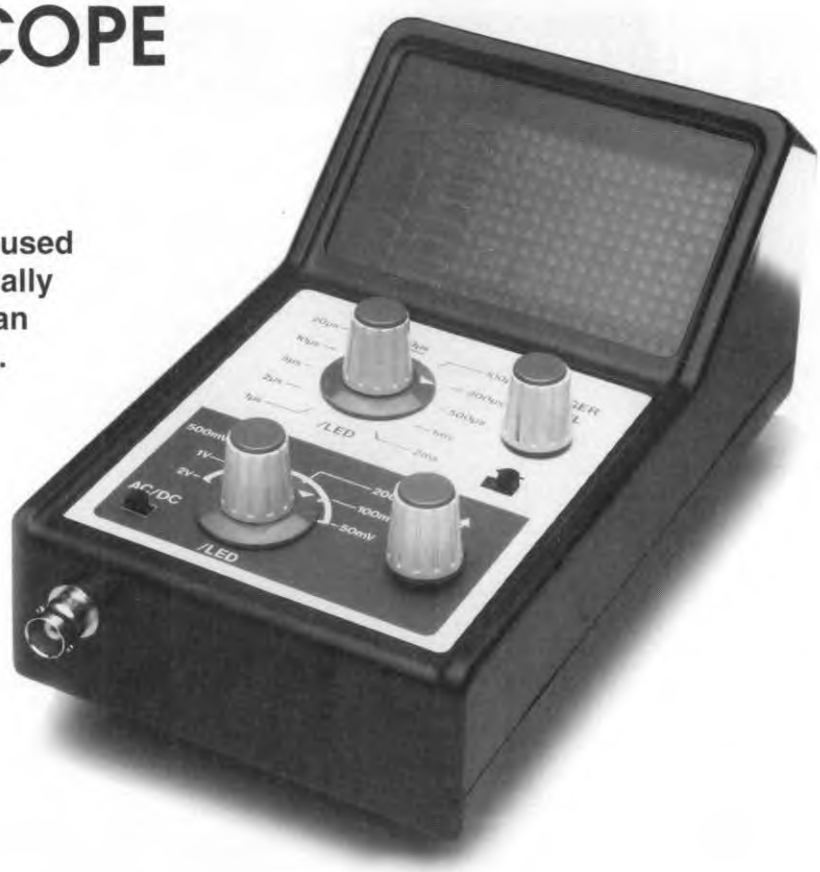
# LED OSCILLOSCOPE

Design by A. Rietjens



**This inexpensive oscilloscope can be used at frequencies up to 20–30 kHz (optionally up to 1 MHz). It works from 12 V and can thus be used as a portable instrument.**

The cost of the oscilloscope is kept down by the use of 3-mm LEDs instead of a cathode ray tube (CRT). These standard LEDs can be bought (in quantity) for between 5p and 8p each (in UK).

The LED matrix that produces the image is shown in **Fig. 1**. The horizontal grid lines represent the *X*-axis (or time base) of the oscilloscope and the vertical ones, the *Y*-axis. A given waveform, say, a sine wave, is shown by making a number of LEDs light in succession. The inertia of the human eye makes it appear as if all the relevant LEDs light.

The lighting of the LEDs is controlled by transistors $T_1$–$T_{10}$, buffers (line drivers) $IC_1$ and $IC_2$, and the circuit shown in **Fig. 2**.

If $D_{151}$ is required to light, $T_1$ must conduct and pin 11 of $IC_2$ must go low. The anode of the diode is then supplied with +10 V via the transistor, while its cathode is earthed via $IC_2$. Series resistor $R_1$ limits the current through the diode. The circuits in **Fig. 2** ensure that only one transistor can conduct, and that only one of the outputs of $IC_1$ and $IC_2$ can become low, at any one time. It is thus impossible for more than one LED to light at any one time.

One of transistors $T_1$–$T_{10}$ is made to conduct by making the relevant base low, while one of the outputs of $IC_1$, $IC_2$ is made low by making the relevant input high. The control voltages for this are pro-

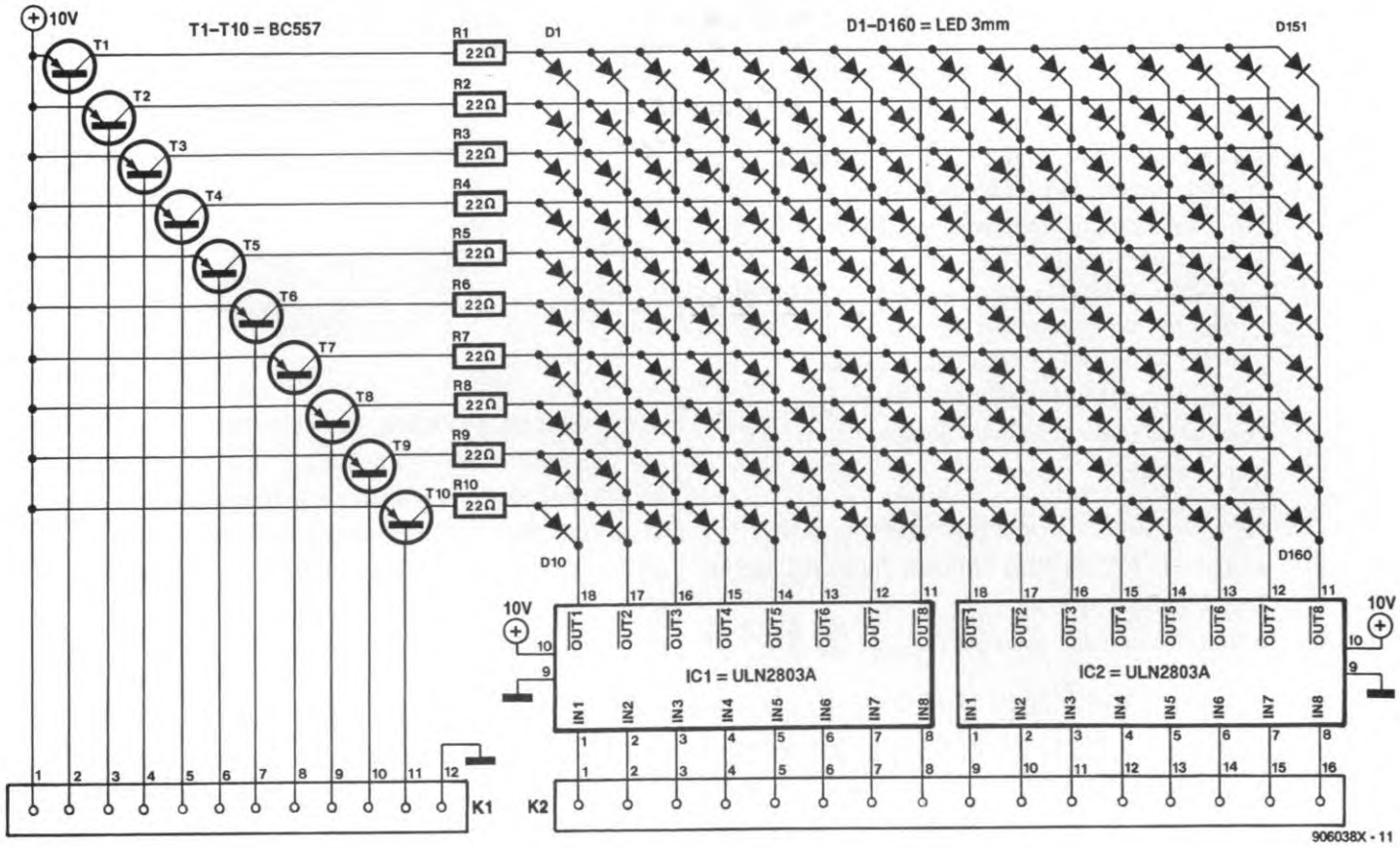



**Fig. 1. The trace of the oscilloscope is produced by a matrix of LEDs of which only one is on at any one time.**

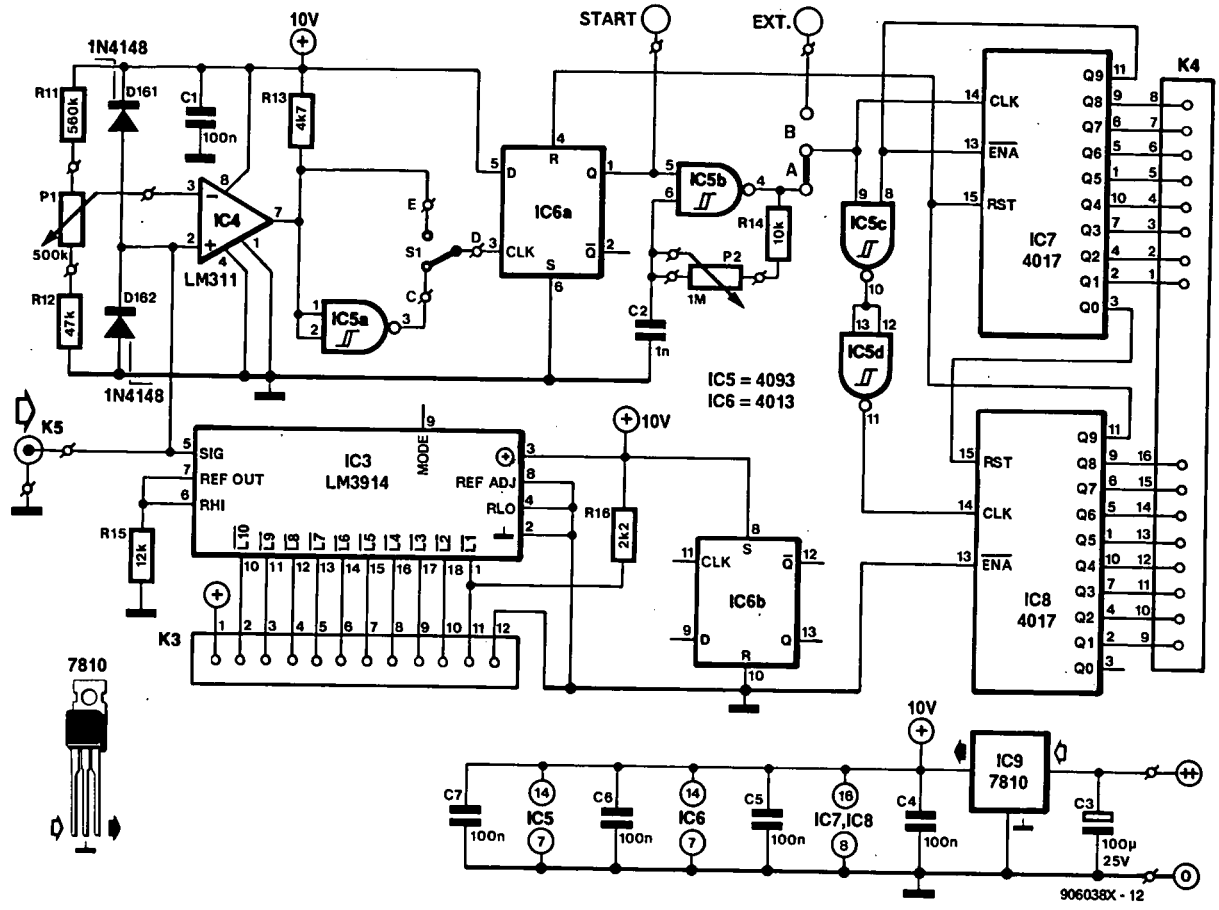



Fig. 2. Drive circuit for the LED matrix.

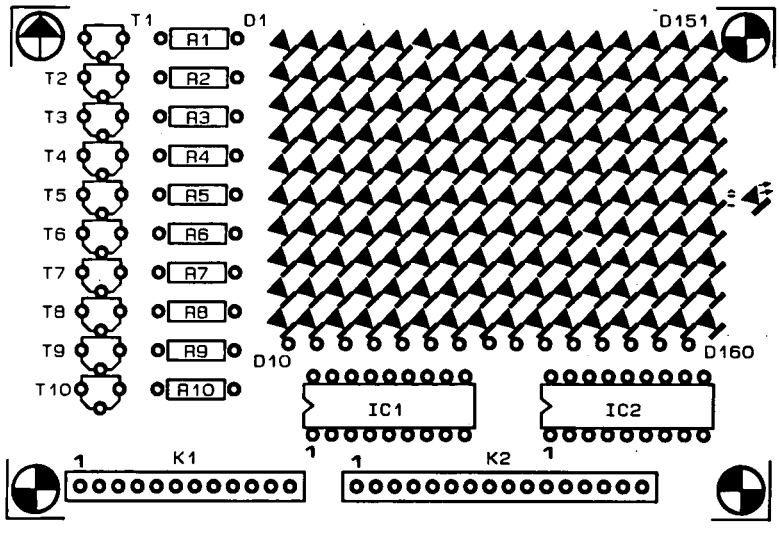



Fig. 3. Printed circuit for the display board (not available ready made).

vided by the circuit in **Fig. 2** via connectors $K_1$ and $K_2$.

## Y-axis

As already stated, the amplitude of the input signal (the measurand) is represented by a vertical 'deflection'. Thus, for a large measurand, one of the upper row of LEDs must light, for a smaller signal, one of a lower row of diodes. This is arranged by analogue-to-digital (A-D) converter $IC_3$ in **Fig. 2**.

When a slowly increasing signal is applied to the SIG input (pin 5) of $IC_3$, outputs $L_1$–$L_{10}$ of this IC go low sequentially, one at a time. This means that when the signal level at pin 5 is low, $L_1$ is low, when the input is high (1.25 V), $L_{10}$ is low, and when the level is somewhere between these values, say, 0.6 V, $L_5$ or $L_6$ is low.

Since the input level must be 0–1.25 V, a signal amplifier/attenuator is required prior to $K_5$ and this will be described a little later on in the article.

## X-axis

The horizontal trace is provided by (decade) counters $IC_7$ and $IC_8$ in **Fig. 2**. Control of the matrix LEDs is from outputs $Q_1$–$Q_8$ of these ICs via $IC_1$ and $IC_2$. The counters

are in series and connected, with the aid of $IC_{5c}$ and $IC_{5d}$, to form a 16-counter.

To make the Q-outputs high, one by one, starting with $Q_1$ of $IC_7$ and ending with $Q_8$ of $IC_8$, clock pulses must be applied to the CLK inputs of both ICs. To ensure that the process proceeds as indicated, the clock to $IC_8$ is interrupted by $IC_{5c}$-$IC_{5d}$ when one of the Q-outputs of $IC_7$ is high. Only when pin 8 of $IC_{5c}$ is high, are clock pulses applied to $IC_8$; they are applied to $IC_7$ at all times.

Because $Q_9$ of $IC_7$ is connected to its own ENA(ble) input and to pin 8 of $IC_{5c}$, as soon as this output is high, $IC_7$ is disabled and clock pulses are applied to $IC_8$. When $Q_8$ of $IC_8$ becomes high, $IC_7$ is reset, whereupon its $Q_0$ goes high, which causes $IC_8$ to be reset also. This is shown on the matrix by the LEDs lighting, one by one, from left to right.

## Clock

The clock pulses for $IC_7$ and $IC_8$ are provided by rectangular-wave generator $IC_{5b}$. The generator is enabled only when its pin 5 is high. Its operation depends on $C_2$ being charged (when pin 4 is high) and discharged (when pin 4 is low) alternately via $R_{14}$-$P_2$. Since the gate is arranged as an inverter, pin 4 is high when pin 6 is low and low when pin 6 is high.

When the level of the potential across $C_2$ approaches that at pin 4, the output of the generator instantly changes state. This means that if the capacitor was being charged (discharged) just prior to the change of state, it will be discharged (charged) after the change. Since this is a continuous action, the output of the generator consists of a train of rectangular pulses whose repetition rate (frequency) depends on the setting of $P_2$.

## Trigger circuit

When the clock generator runs continuously, a still trace is obtained only if the frequency of the input signal is the same as that at which horizontal deflection takes place, or a whole multiple of it.

Since the input frequency is better not, or cannot be, altered, the horizontal deflection frequency must be variable. In **Fig. 2**, this is made possible by $P_2$. None the less, because of changes in temperature and other factors, one or both of the frequencies will shift to some extent. This will result in a trace that constantly moves across the screen.

It is thus necessary to ensure that the input frequency and the deflection frequency are synchronized at all times. As is normal, this is achieved by triggering the time base with the input signal. To that end, part of the input signal is applied to pin 2 of $IC_4$ (the trigger circuit consists of $IC_4$, $IC_5$, and $IC_{6a}$).

To ensure that the input levels of $IC_3$ and $IC_4$ are not exceeded, the signal input is provided with a voltage limiter consisting of series-connected diodes $D_{161}$ and $D_{162}$. The supply voltage exists across this series network, but no current flows through this, because the diodes are inverse-biased. When the level at the input exceeds 10.6 V, $D_{161}$ begins to conduct; when the input drops below –0.6 V, $D_{162}$ begins to conduct. This means that the diodes limit the range of input levels to between 0.6 V below earth potential and 0.6 V above the supply voltage.

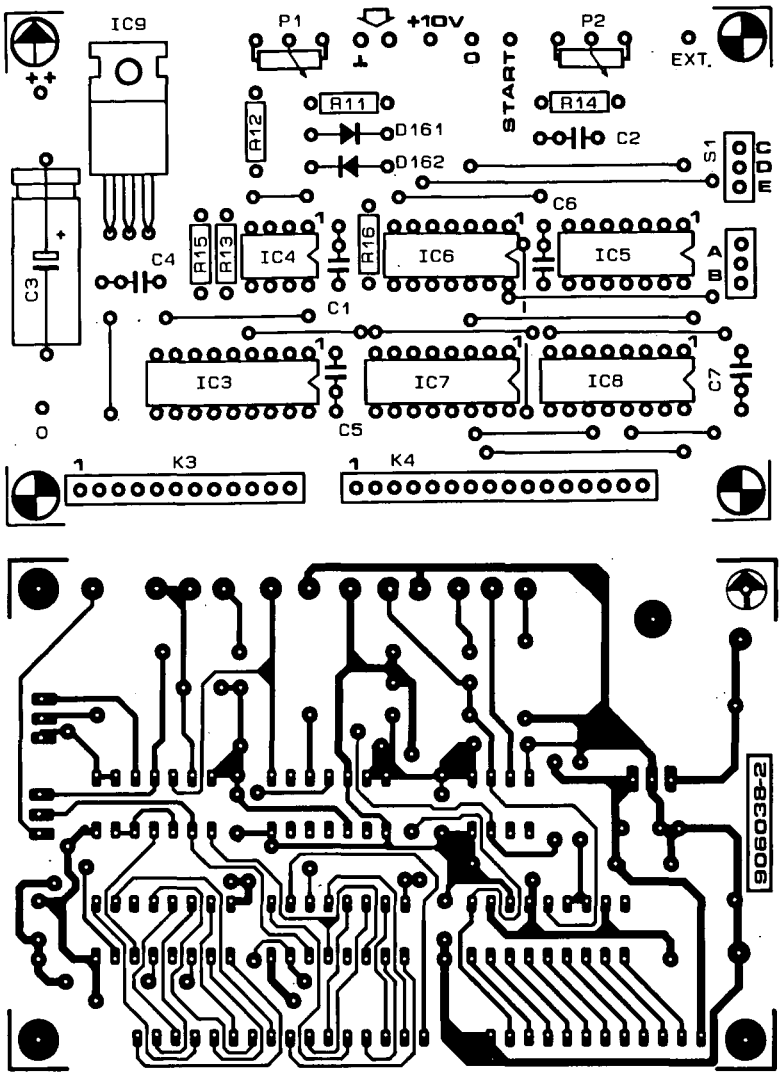



**Fig. 4. Printed circuit for the driver board (not available ready made).**

Circuit $IC_4$ is arranged as a comparator, that is, there is no feedback resistor between its output (pin 7) and its inverting input (pin 3). This means that, in theory, the amplification of the opamp is infinite, so that the level of its output voltage can only be 0 V (earth potential) or 10 V (supply voltage). The output cannot be set to any intermediate value. In other words, if the level of the signal at pin 2 rises above a certain value, the output instantly becomes 10 V; if the level drops below that certain value, the output immediately becomes 0 V. The value at which this happens, the change-over or toggle point, is set with $P_2$.

Since the output of $IC_4$ is thus either 10 V or 0 V, even for very small input signals, any input is converted into a rectangular voltage, whose frequency is identical to that of the input signal. This means that the output is synchronous with the input signal.

The output of $IC_4$ is used to trigger clock generator $IC_{5b}$ at exactly the right moment via D-bistable $IC_{6a}$. When $IC_4$ applies a clock pulse to $IC_{6a}$, the Q-output of this stage goes high, whereupon $IC_{5b}$ is enabled. Switch $S_1$, in conjunction with inverter $IC_{5a}$, determines whether the clock is enabled at the leading or at the trailing edge of the input signal. The exact instant of onset of the trace is set with preset $P_1$.

When decade counters $IC_7$ and $IC_8$ reach their maximum counter state, they are reset to their starting state via $Q_9$ of $IC_8$; $IC_6$ is then also reset, so that the clock generator is disabled. The clock is reenabled at the next output of $IC_4$. If, therefore, there is no input signal, the LEDs are out, because there is no trigger.

## Construction

The oscilloscope is constructed on two printed-circuit boards, one for the display (**Fig. 3** and **5**) and the other for the driver (**Fig. 4**, **6**, and **7**).

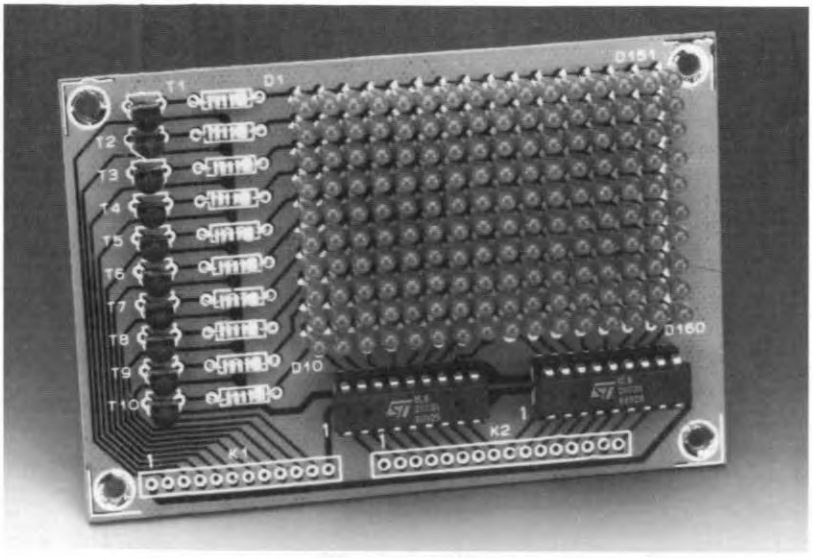



Fig. 5. Completed display board (component side).

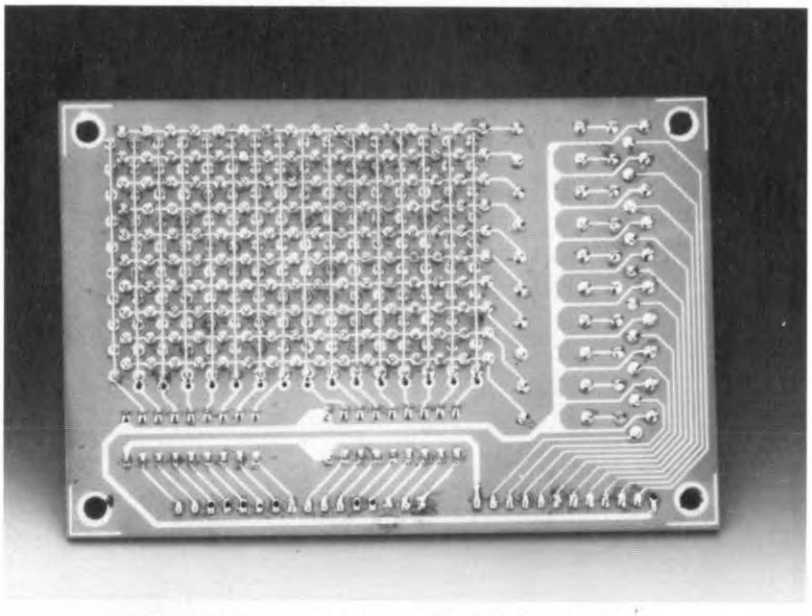


Fig. 6. Completed display board (track side).

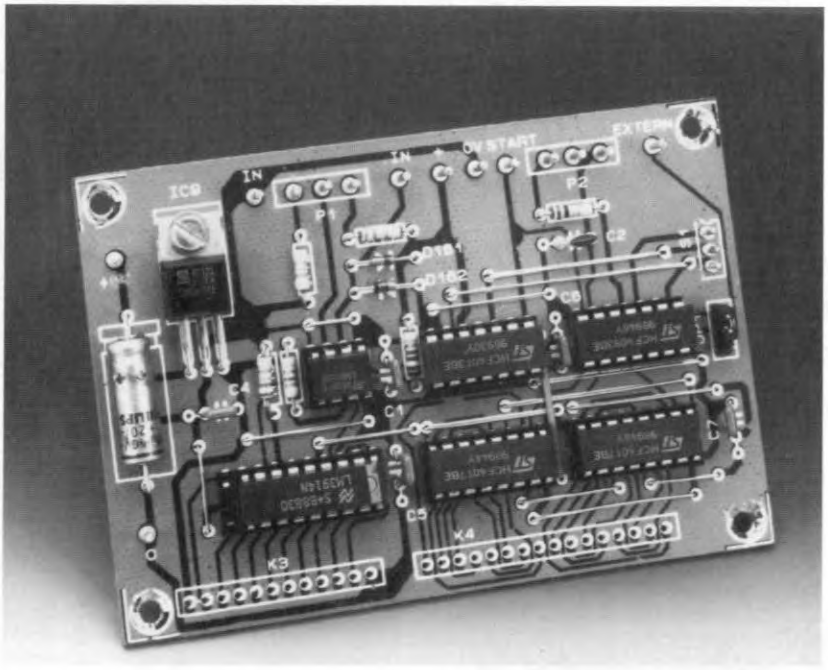



Fig. 7. Completed driver board (component side).

The cathodes of each row of LEDs must be linked via a suitable length of wire which remains suspended above the track side of the board and is connected to the relevant pin of $IC_1$ and $IC_2$—see **Fig. 1**. The anodes are soldered directly to the board.

Finishing the boards is straightforward. Since the two boards are the same size, they may be assembled into a 'sandwich' with the aid of suitable spacers.

## Optional attenuator/amplifier

The single input voltage range of the oscilloscope may be extended to six ranges with an optional attenuator/amplifier. Both the attenuation and amplification factors are well defined to ensure accurate measurements. Furthermore, both are as nearly frequency-independent as possible. The unit described is usable at frequencies up to 40 kHz.

The circuit of the unit is shown in **Fig. 8**: the (variable) attenuator is formed by switch $S_3$ and resistors $R_{17}$–$R_{24}$. The remainder of the circuit functions as a differential amplifier.

With $S_2$ open, $C_8$ prevents any direct voltage at the input entering the circuit. This is useful if, for instance, the ripple on a supply voltage is to be measured.

The values of resistors $R_{17}$–$R_{24}$ have been chosen to provide six ranges of sensitivity as shown in **Table 1**.

Operational amplifiers $IC_{10}$ and $IC_{11}$ form a differential ×4 amplifier. Since they are supplied with a positive voltage only and the input signal can be negative, the input levels are shifted. This is achieved by linking the earthy input connection not to supply earth, but to a point halfway between the supply earth and +10 V, that is, to +5 V (since $R_{25}$ and $R_{26}$ have identical values). This means that the input voltage alternates around +5 V.

Operational amplifiers $IC_{10a}$ and $IC_{10b}$ are protected against too high inputs by diodes $D_{163}$–$D_{166}$. If the level at the 'earthy' input pin rises above +10 V, $D_{163}$ conducts, whereas if it drops below 0 V, $D_{164}$ conducts. Diodes $D_{165}$ and $D_{166}$ function similarly when the level at the upper input terminal rises above 10 V or drops below 0 V respectively.

The potential difference across the input pins is amplified at the outputs of

| Position $S_3$ | Sensitivity (volt per LED) |
|---|---|
| 1 | 2 |
| 2 | 1 |
| 3 | 0.5 |
| 4 | 0.2 |
| 5 | 0.1 |
| 6 | 0.05 |

Table 1.

$IC_{10a}$ and $IC_{10b}$, from where it is applied to the –ve and +ve inputs of $IC_{11}$. This circuit sums the two voltages which are then applied to the input of the oscilloscope.

The level of the d.c. component at the output (pin 6) of $IC_{11}$ is set with $P_3$, which means that the waveform on the oscilloscope can be shifted vertically with $P_3$.

Since the level at the input of the oscilloscope must not exceed +1.2 V, diodes $D_{167}$ and $D_{168}$ conduct when the output of $IC_{11}$ rises above 1.2 V. Note that the output cannot become negative, because the supply of the opamp is 0 (earth) to +10 V.

**Construction**. The unit is best built on the printed-circuit board shown in **Fig. 9** and **10**: note, however, that this is not available ready made. Switch $S_3$ and potentiometer $P_3$ must be soldered directly to the board.

Since the 'apparent earth' of the input terminals floats 5 V above real earth, only the input terminals are accessible from outside, the real earth is not.

The unit is best tested in conjunction with the oscilloscope. Apply a variable alternating voltage to the input of the attenuator/amplifier and check that six different sensitivities can be selected with $S_3$. Rotating $P_3$ should shift the trace on the oscilloscope vertically.

## More accurate time base

The on-board time base of the oscilloscope is intended for applications where the accent is more on viewing waveforms than on accurate measurements. If, however, not only the waveform, but also the frequency (or period) of a certain signal is to be assessed, a more accurate time base is required. In an oscilloscope, an unknown frequency is measured by comparing it with a known frequency: that of the time base generator. It is clear that the time base frequency must be accurate if it is to function as a reference. In the present time base a fixed 1 MHz generator is used, which is followed by a variable divider, so that not only 1 µs pulses, but also longer ones, are available.

The time base circuit is shown in **Fig. 11**. The 1 MHz clock is formed by

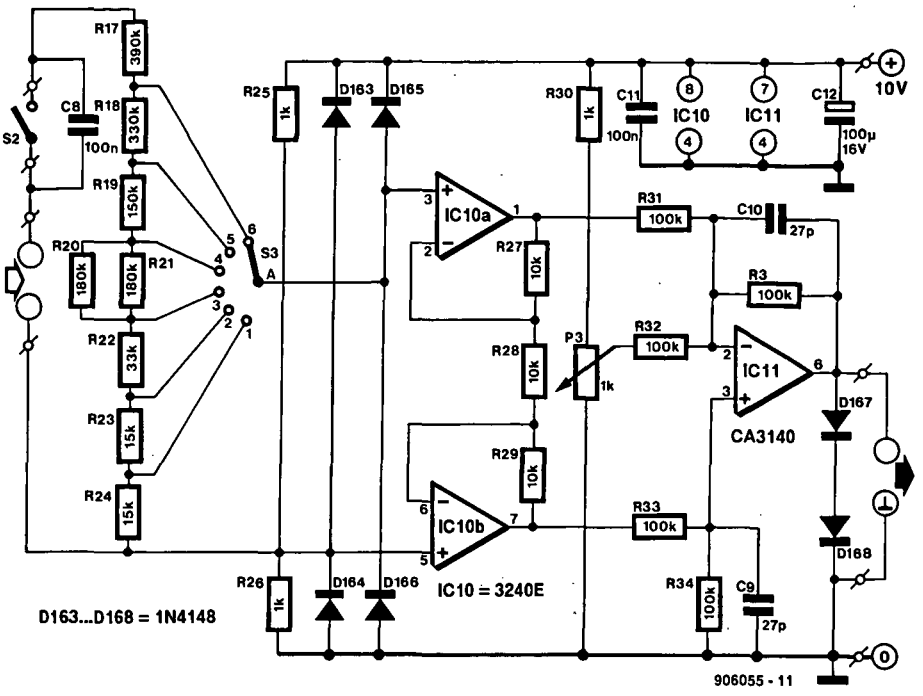



Fig. 8. Circuit diagram of the (optional) attenuator/amplifier.

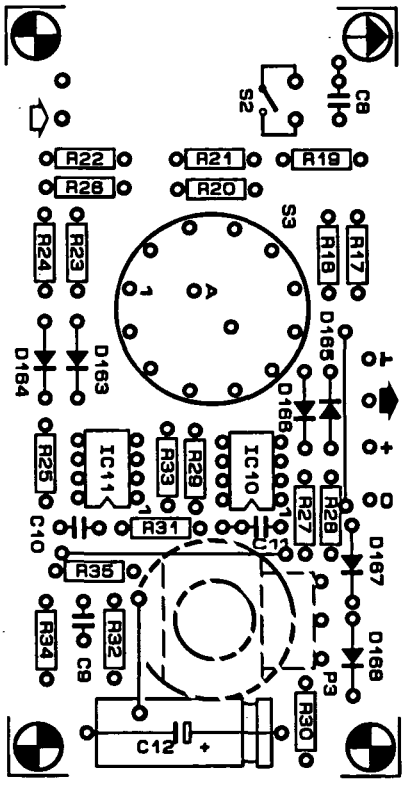
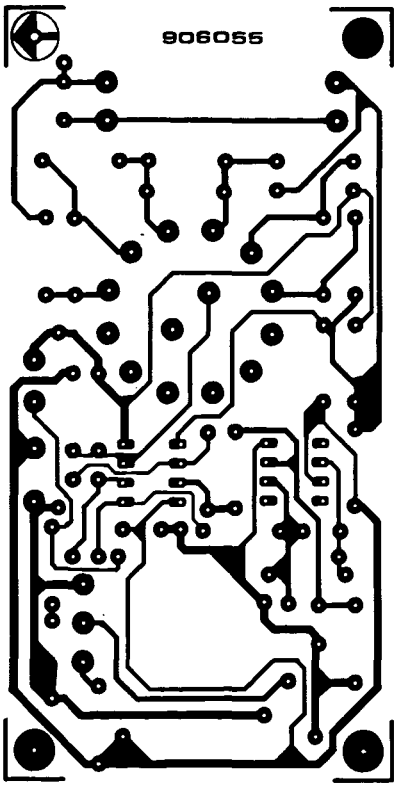



Fig. 9. Printed-circuit board for the attenuator/amplifier (not available ready made).



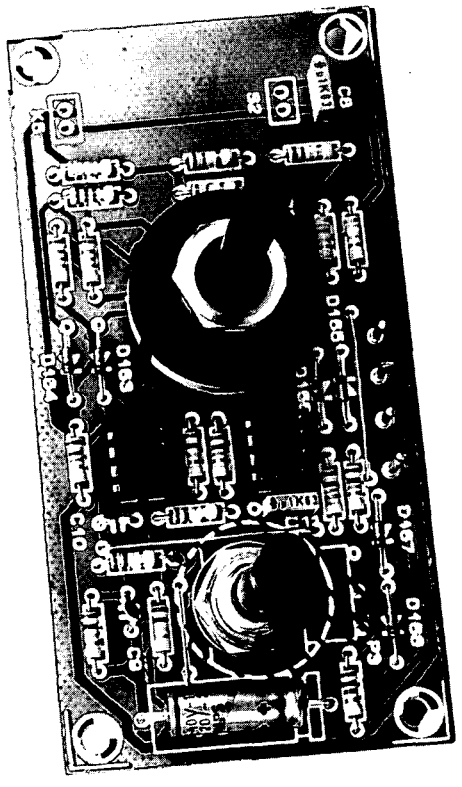



Fig. 10. Completed attenuator/amplifier board.

Schmitt trigger NAND gate $IC_{13a}$. When $C_{14}$ is charged to a certain level, $IC_{13a}$ changes state, whereupon $C_{14}$ is discharged. When it is discharged to a certain level, $IC_{13a}$ again changes state, and the capacitor is charged again. This results in a triangular voltage across the capacitor.

The output of $IC_{13a}$ is a stream of rectangular pulses with a PRR (pulse repetition rate), $f_{ck}$, of 1 MHz, and this is used as the clock for the time base. When the START input of the time base circuit is made high by the oscilloscope, the pulse train is applied to the clock input of divider $IC_{12}$ via $IC_{13d}$.

The 11 dividers (bistables) contained in $IC_{12}$ are cascaded. The construction of each bistable is such that upon each high-low transition at its input, its output changes state. That is, at the first high, the divider is set, at the second, it is reset, at the third, it is set again, and so on. This means that a rectangular signal is divided by two, so that the frequency at the output of the bistable is half that at its input. If $IC_{12}$ were considered on its own, the frequency at $Q_0$ would be $f_{ck}/2$, that at $Q_1$, $f_{ck}/4$, and that at $Q_{10}$ $f_{ck}/2048$. Thus, as long as there is a clock signal at pin 10, all binary combinations between 000 0000 0000 and 111 1111 1111 would be available.

However, although the bistables in $IC_{12}$ are set at a high-low transition at their input, they are reset immediately after being set (upon their output going high). Therefore, at the next high-low transition, the bistable is already reset, so that it is set again. With $S_4$ in position 1, $Q_0$ is set at every high-low transition of the clock pulses, which means that the frequency at $Q_0$ is equal to $f_{ck}$.

The circuit which ensures that a bistable is set and almost immediately reset is the delay network formed by $IC_{13b}$ and $IC_{13c}$. The reset pulses are provided by the selected Q output, relevant diodes and $S_4$. For example, when the first divider is set, $Q_0$ goes high and this high level is transferred immediately via $S_4$, $IC_{13b}$ and $IC_{13c}$ to the reset input of $IC_{12}$, whereupon $Q_0$ becomes low again. This process results in a very short pulse at the EXT output, which is used to set the decoders on the mother board to their next state.

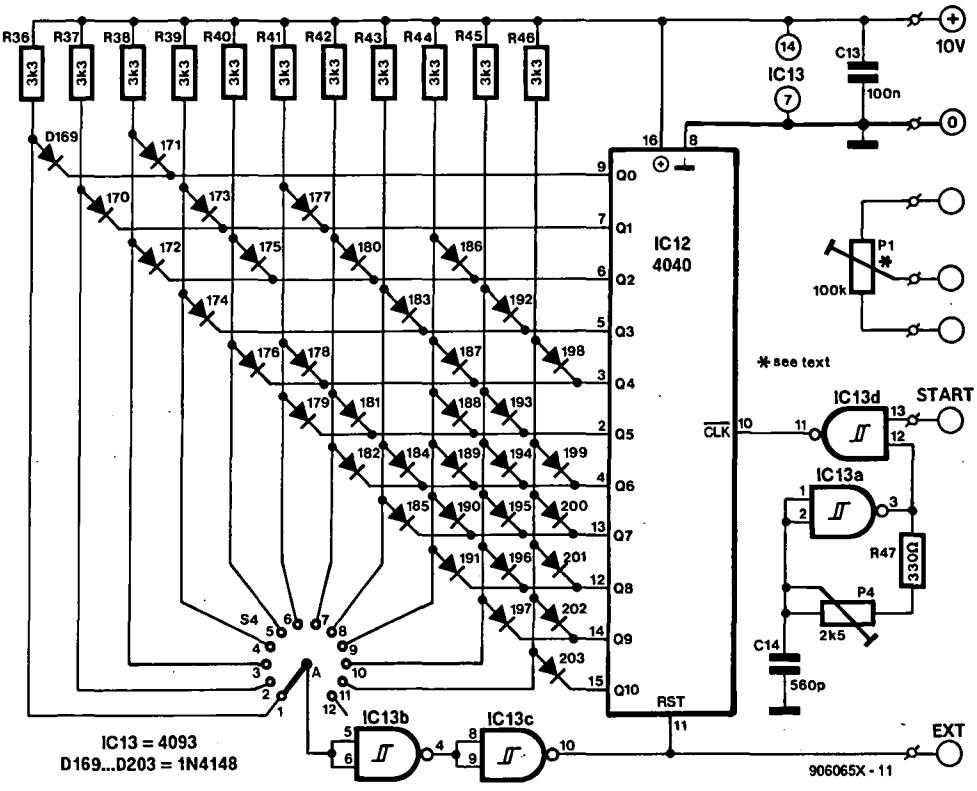



Fig. 11. Circuit diagram of the time base.

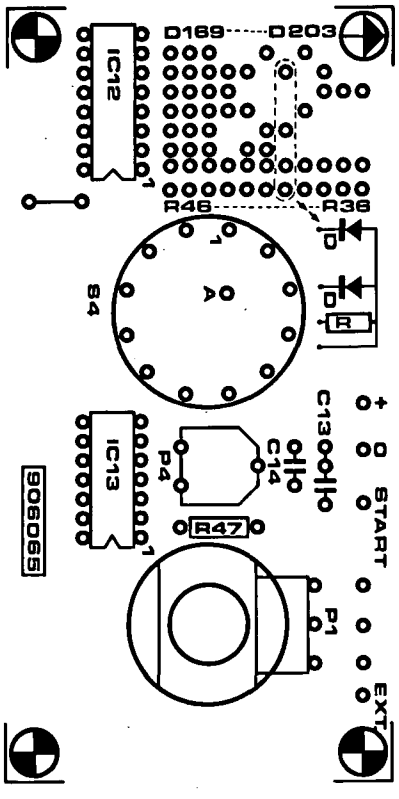
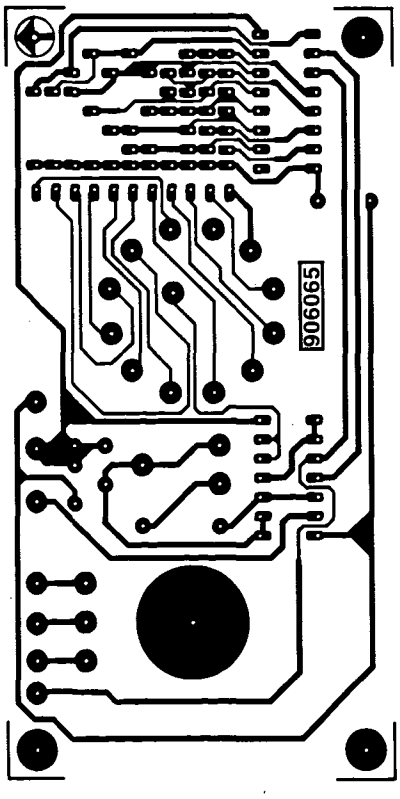



Fig. 12. Printed-circuit board for the time base (not available ready made).



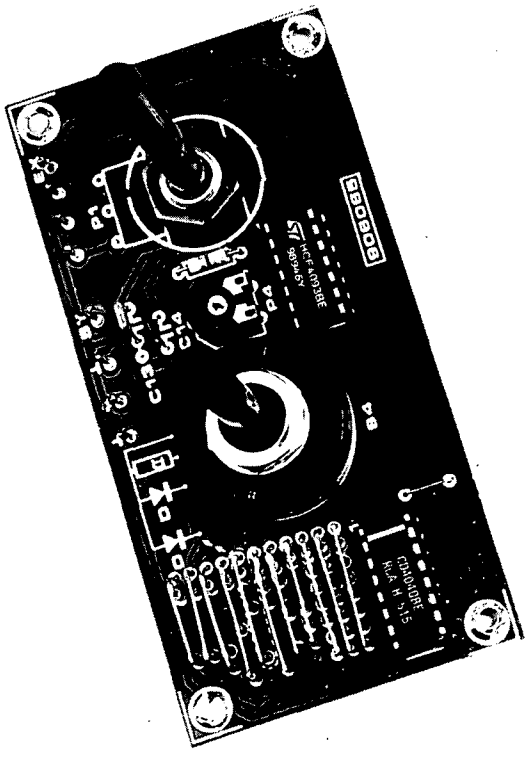



Fig. 13. Completed printed-circuit board for the time base.

**Diode matrix**. The input of the delay network is connected to the Q outputs of $IC_{12}$ via a diode matrix. This matrix ensures that $IC_{12}$ does not always have to go through all its counter states, but is reset, that is taken back to zero, after a given number of states. As mentioned before, $IC_{12}$ is reset by the pulse provided by the relevant Q output and diodes, and $S_4$. Thus, the diode matrix, in conjunction with $S_4$, ensures that resetting takes place only when certain binary codes (numbers) exist on the Q outputs.

For example, with $S_4$ in position 1, the divider can count only to 1: in **Fig. 11**, the input of the delay network is connected only to $Q_0$ (via $S_4$ and $D_{169}$). This means that $IC_{12}$ is reset almost immediately: the binary number at its Q outputs is then 000 0000 0001. When $S_4$ is in position 2, $IC_{12}$ is reset when $Q_1$ goes high: counter position 000 0000 0010. With $S_4$ in position 3, $Q_0$ and $Q_2$ must be high simultaneously before a reset pulse is generated.

Since the position of $S_4$ determines when a reset of $IC_{12}$ takes place, it also determines at what intervals the time base generates short pulses at the EXT output. The diode matrix has been designed to provide intervals in the ratio 1:2:5, that is, 1 µs, 2 µs, 5 µs, 10 µs, 20 µs, 50 µs, 100 µs, 200 µs, 500 µs, 1 ms and 2 ms.

Preset $P_1$ is the trigger control already discussed in the section 'Trigger circuit'.

**Construction**. The time base circuit is best built on the printed-circuit board in **Fig. 12**, which is, however, not available ready made. The finished board is shown in **Fig. 13**.

Test the circuit by applying a 10 V supply to it and holding it near a MW receiver: the 1 MHz clock should be heard clearly.

**Assembly**. The four boards and a suitable enclosure for them are shown in **Fig. 14**. A suitable (not mandatory) way of fitting the boards in the case is illustrated in **Fig. 17**. Other types of assembly are, of course, possible. A suggested front panel is shown in **Fig. 15**.

The interconnections between the boards are shown in the diagram in **Fig. 16**. Do not forget to place the wire bridge at the EXT connection on the driver board to position B.

If the original clock on the driver board is not intended to be used, $P_2$ may be omitted.

All wires carrying analogue signals should be single screened cables with the screen earthed at one end only. This applies particularly to the signal input, the attenuator/amplifier and the circuit around $IC_4$ on the driver board.

All earth wires between the boards should be separate wires.

Before the case can be closed, set the clock generator to exactly 1 MHz with $P_4$, which is best done with the aid of a frequency counter.

## Parts list

***Display board***

**Resistors**:
$R_1$–$R_{10}$ = 22 Ω

**Semiconductors**:
$T_1$–$T_{10}$ = BC557
$D_1$–$D_{160}$ = LED, 3 mm, red

**Integrated circuits**:
$IC_1$, $IC_2$ = ULN2803A

***Driver board***

**Resistors**:
$R_{11}$ = 560 kΩ
$R_{12}$ = 47 kΩ
$R_{13}$ = 4.7 kΩ
$R_{14}$ = 10 kΩ
$R_{15}$ = 12 kΩ
$R_{16}$ = 2.2 kΩ
$P_1$ = 500 kΩ linear potentiometer
$P_2$ = 1 MΩ logarithmic potentiometer

**Capacitors**:
$C_1$, $C_4$–$C_7$ = 100 nF
$C_2$ = 1 nF
$C_3$ = 100 µF, 25 V

**Semiconductors**:
$D_{161}$, $D_{162}$ = 1N4148

**Integrated circuits**:
$IC_3$ = LM3914
$IC_4$ = LM311

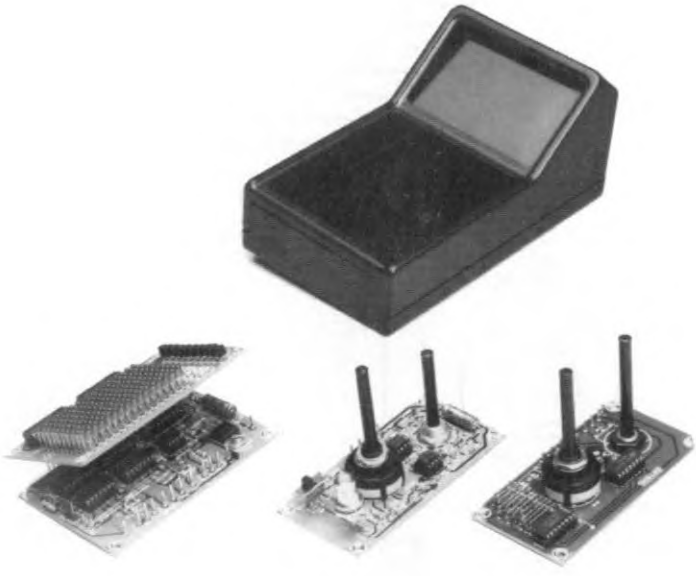


Fig. 14. The constituents of the oscilloscope.

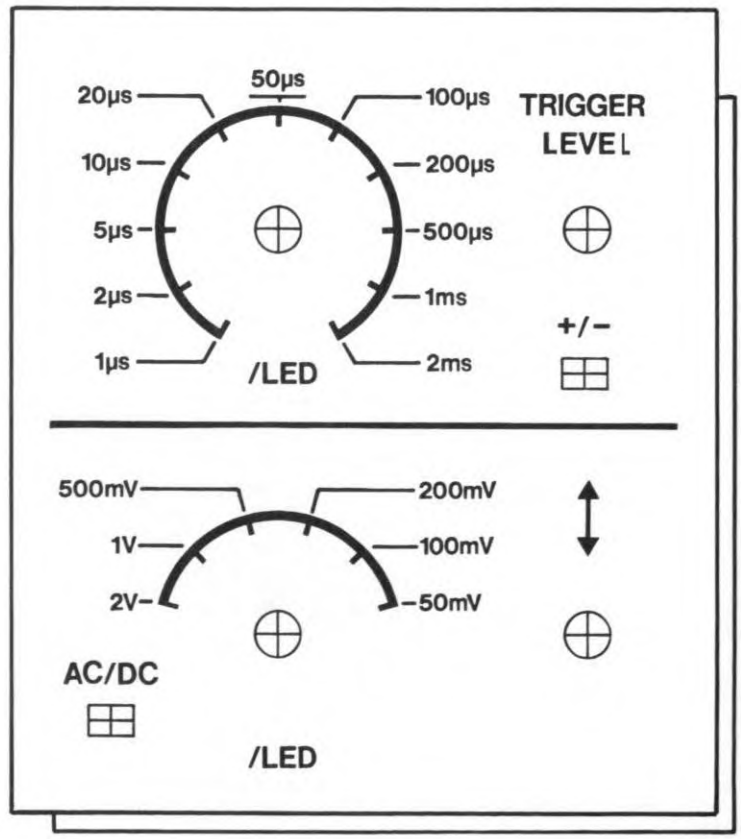



Fig. 15. Suggested front panel layout for the oscilloscope.

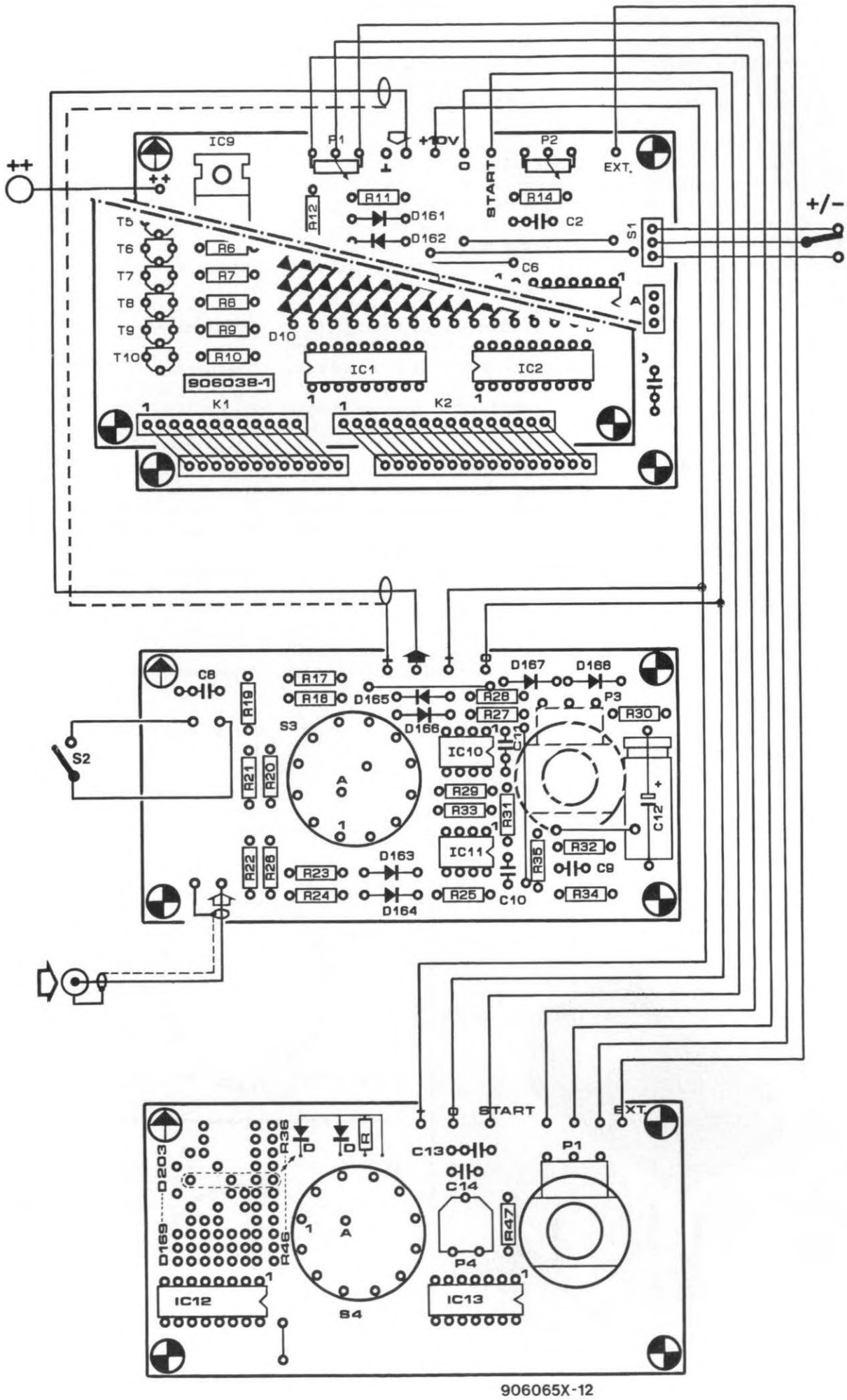



Fig. 16. Interwiring diagram for the complete oscilloscope.

$IC_5$ = 4093
$IC_6$ = 4013
$IC_7$; $IC_8$ = 4017
$IC_9$ = 7810

**Miscellaneous**:
$S_1$ = single-pole change-over switch

***Attenuator/amplifier***

**Resistors**:
$R_{17}$ = 390 kΩ
$R_{18}$ = 330 kΩ
$R_{19}$ = 150 kΩ
$R_{20}$, $R_{21}$ = 180 kΩ
$R_{22}$ = 33 kΩ
$R_{23}$, $R_{24}$ = 15 kΩ
$R_{25}$, $R_{26}$, $R_{30}$ = 1 kΩ
$R_{27}$–$R_{29}$ = 10 kΩ
$R_{31}$–$R_{35}$ = 100 kΩ
$P_3$ = 1 kΩ linear potentiometer

**Capacitors**:
$C_8$; $C_{11}$ = 100 nF
$C_9$; $C_{10}$ = 27 pF
$C_{12}$ = 100 µF, 16 V

**Semiconductors**:
$D_{163}$–$D_{168}$ = 1N4148

**Integrated circuits**:
$IC_{10}$ = CA3240E
$IC_{11}$ = CA3140

**Miscellaneous**:
$K_5$ = BNC connector
$S_2$ = single-pole on-off switch
$S_3$ = 2-pole, 6-position rotary switch

***Time base***

**Resistors**:
$R_{36}$–$R_{46}$ = 3.3 kΩ
$R_{47}$ = 330 Ω
$P_4$ = 2.5 kΩ preset

**Capacitors**:
$C_{13}$ = 100 nF
$C_{14}$ = 560 pF

**Semiconductors**:
$D_{169}$–$D_{203}$ = 1N4148

**Integrated circuits**:
$IC_{12}$ = 4040
$IC_{13}$ = 4093

**Miscellaneous**:
$S_4$ = 1-pole, 12-position rotary switch
Enclosure: Suggested Bopla BP 680 (available from Phoenix Mecano, phone (0296) 398 855; fax (0296) 398 866

[906038-55-65]

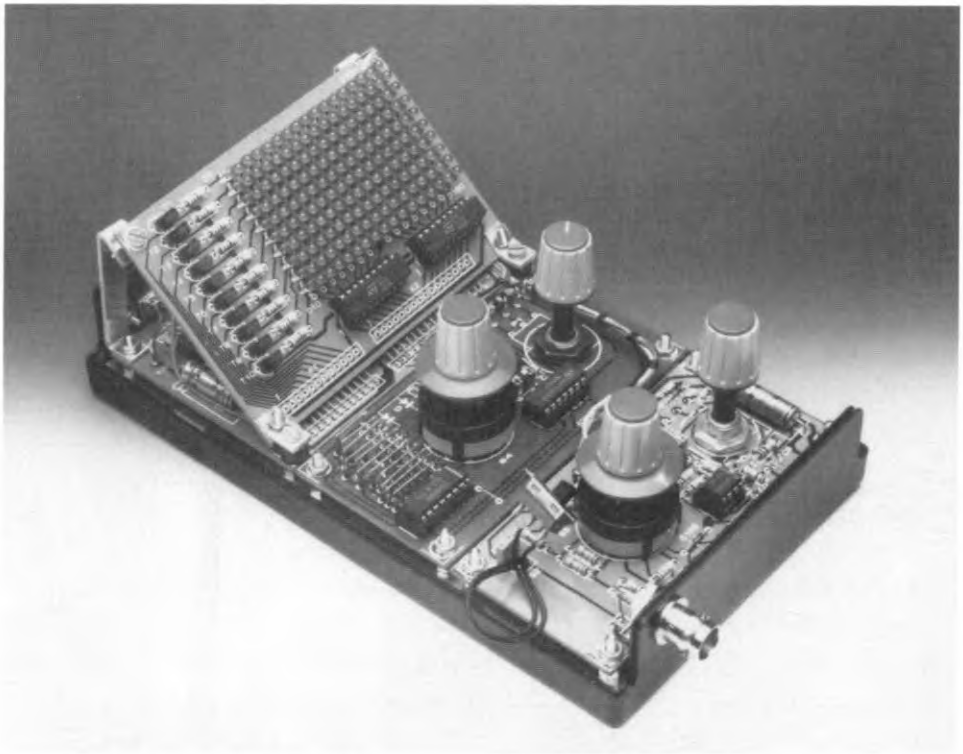


**Fig. 17. Suggested assembly of the complete oscilloscope.**